High Speed, Dual, 4 A MOSFET Driver

Data Sheet

ADP3654

FEATURES

- Industry-standard-compatible pinout
- High current drive capability
- Precise UVLO comparator with hysteresis
- 3.3 V-compatible inputs
- 10 ns typical rise time and fall time at 2.2 nF load
- Matched propagation delays between channels
- Fast propagation delay
- 4.5 V to 18 V supply voltage
- Parallelable dual outputs
- Rated from −40°C to +125°C junction temperature
- Thermally enhanced packages, 8-lead SOIC_N_EP and 8-lead MINI_SO_EP

APPLICATIONS

- AC-to-dc switch mode power supplies
- DC-to-dc power supplies
- Synchronous rectification
- Motor drives

GENERAL DESCRIPTION

The ADP3654 high current and dual high speed driver is capable of driving two independent N-channel power MOSFETs. The driver uses the industry-standard footprint but adds high speed switching performance.

The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers.

Digital power controllers are powered from a low voltage supply, and the driver is powered from a higher voltage supply. The ADP3654 driver adds UVLO and hysteresis functions, allowing safe startup and shutdown of the higher voltage supply when used with low voltage digital controllers.

The driver is available in thermally enhanced SOIC_N_EP and MINI_SO_EP packaging to maximize high frequency and current switching in a small printed circuit board (PCB) area.

FUNCTIONAL BLOCK DIAGRAM

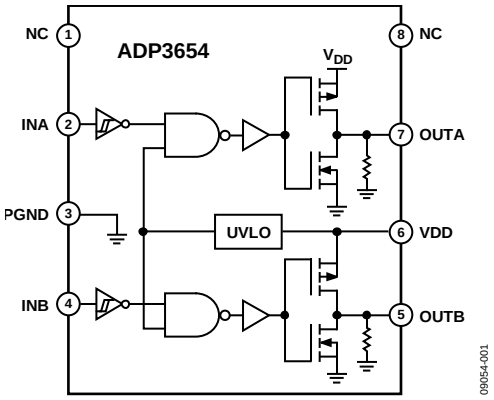

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support
www.analog.com

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8/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 12 V, T_J = −40°C to +125°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range	V_{DD}		4.5		18	V
Supply Current	I_{DD}	No switching		1.2	3	mA
UVLO						
Turn-On Threshold Voltage	V_{UVLO_ON}	V_{DD} rising, T_J = 25°C, see Figure 3	3.8	4.2	4.5	V
Turn-Off Threshold Voltage	V_{UVLO_OFF}	V_{DD} falling, T_J = 25°C, see Figure 3	3.5	3.9	4.3	V
Hysteresis				0.3		V
DIGITAL INPUTS (INA, INB)						
Input Voltage High	V_{IH}	See Figure 2	2.0			V
Input Voltage Low	V_{IL}	See Figure 2			0.8	V
Input Current	I_{IN}	0 V < V_{IN} < V_{DD}	−20		+20	µA
Internal Pull-Up/Pull-Down Current				6		µA
OUTPUTS (OUTA, OUTB)						
Output Resistance, Unbiased		VDD = PGND		80		kΩ
Peak Source Current		See Figure 14		4		A
Peak Sink Current		See Figure 14		−4		A
SWITCHING TIME						
OUTA and OUTB Rise Time	t_{RISE}	C_{LOAD} = 2.2 nF, see Figure 2		10	25	ns
OUTA and OUTB Fall Time	t_{FALL}	C_{LOAD} = 2.2 nF, see Figure 2		10	25	ns
OUTA and OUTB Rising Propagation Delay	t_{D1}	C_{LOAD} = 2.2 nF, see Figure 2		14	30	ns
OUTA and OUTB Falling Propagation Delay	t_{D2}	C_{LOAD} = 2.2 nF, see Figure 2		22	35	ns
Delay Matching Between Channels				2		ns

[1] All limits at temperature extremes guaranteed via correlation using standard statistical quality control (SQC) methods.

TIMING DIAGRAMS

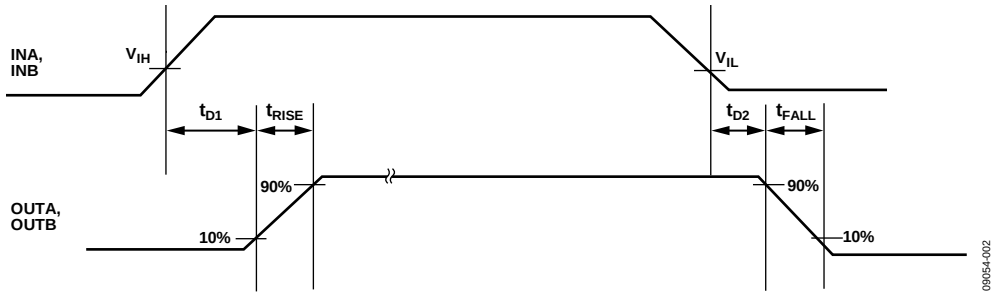

Figure 2. Output Timing Diagram

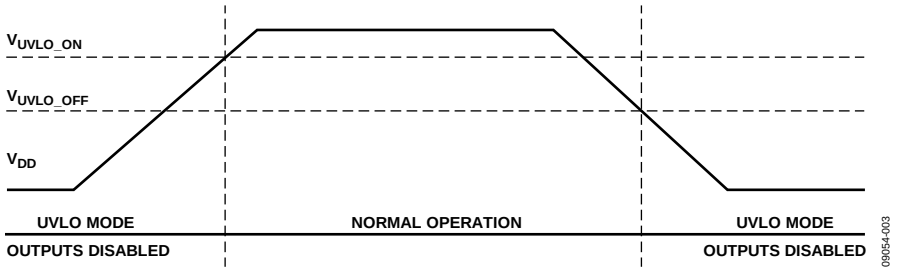

Figure 3. UVLO Function

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDD	−0.3 V to +20 V
OUTA, OUTB	
DC	−0.3 V to V_{DD} + 0.3 V
<200 ns	−2 V to V_{DD} + 0.3 V
INA, INB	−0.3 V to V_{DD} + 0.3 V
ESD	
Human Body Model (HBM)	3.5 kV
Field Induced Charged Device Model (FICDM)	
SOIC_N_EP	1.5 kV
MINI_SO_EP	1.0 kV
θ_{JA}, JEDEC 4-Layer Board	
SOIC_N_EP[1]	59°C/W
MINI_SO_EP[1]	43°C/W
Junction Temperature Range	−40°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	260°C

[1] θ_{JA} is measured per JEDEC standards, JESD51-2, JESD51-5, and JESD51-7, as appropriate with the exposed pad soldered to the PCB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

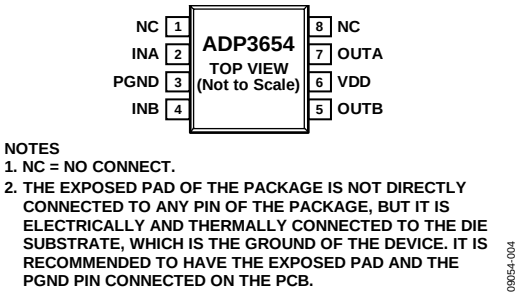

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	INA	Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	NC	No Connect.
9	EPAD	Exposed Pad. The exposed pad of the package is not directly connected to any pin of the package, but it is electrically and thermally connected to the die substrate, which is the ground of the device. It is recommended to have the exposed pad and the PGND pin connected on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12 V, T_J = 25°C, unless otherwise noted.

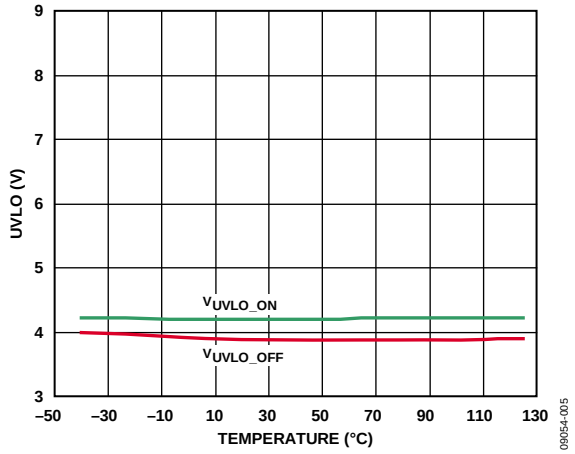

Figure 5. UVLO vs. Temperature

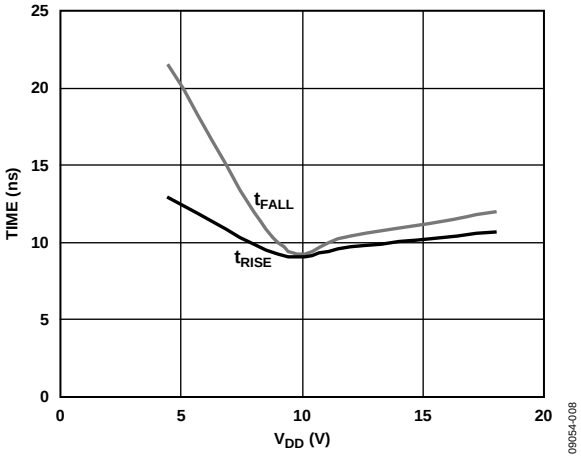

Figure 8. Rise and Fall Times vs. V_{DD}

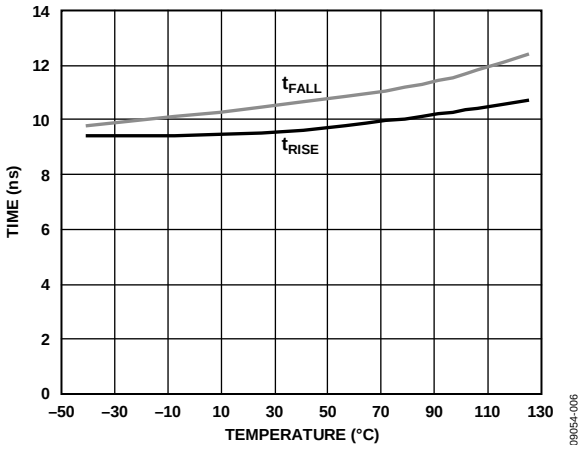

Figure 6. Rise and Fall Times vs. Temperature

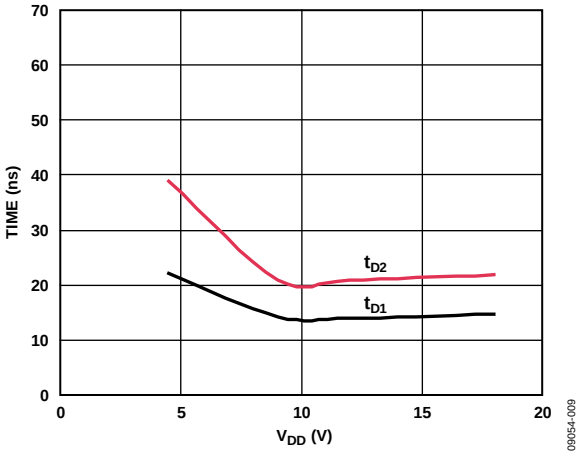

Figure 9. Propagation Delay vs. V_{DD}

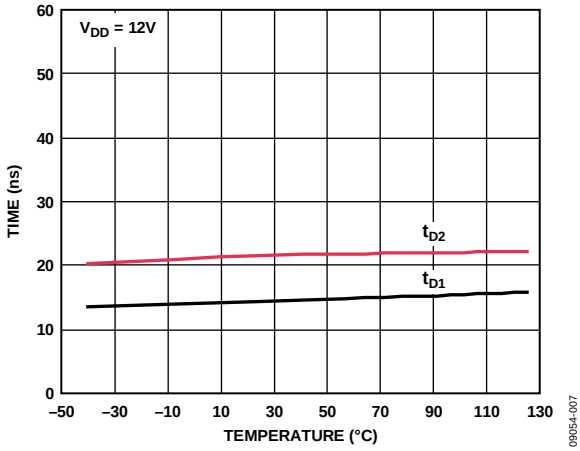

Figure 7. Propagation Delay vs. Temperature

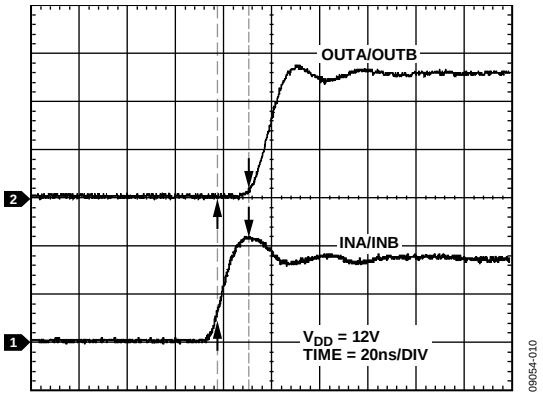

Figure 10. Typical Rise Propagation Delay

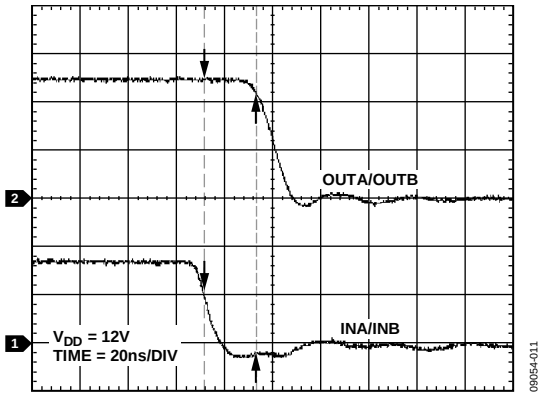

Figure 11. Typical Fall Propagation Delay

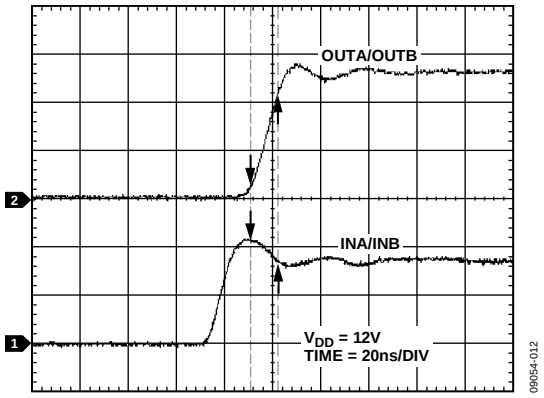

Figure 12. Typical Rise Time

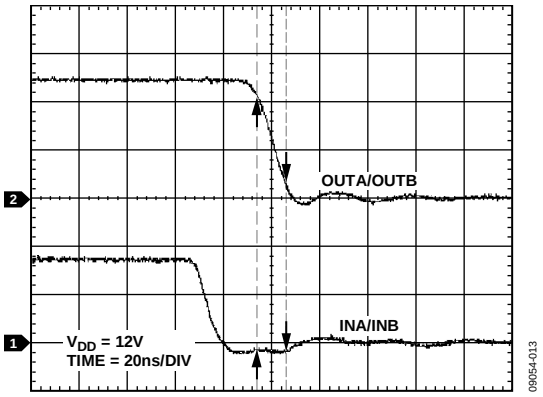

Figure 13. Typical Fall Time

TEST CIRCUIT

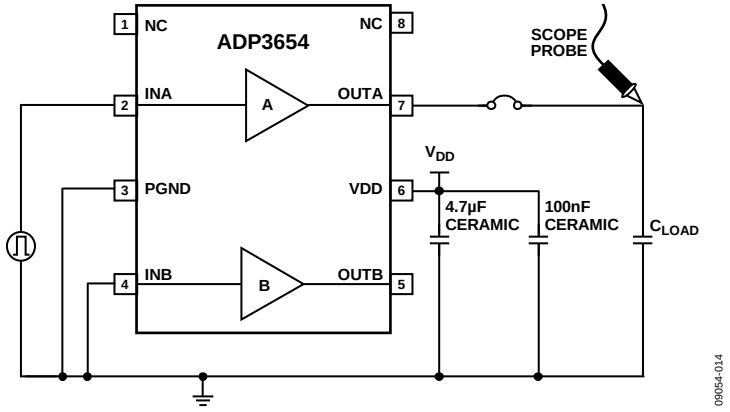

Figure 14. Test Circuit

THEORY OF OPERATION

The ADP3654 dual driver is optimized for driving two independent enhancement N-channel MOSFETs or insulated gate bipolar transistors (IGBTs) in high switching frequency applications.

These applications require high speed, fast rise and fall times, as well as short propagation delays. The capacitive nature of the aforementioned gated devices requires high peak current capability as well.

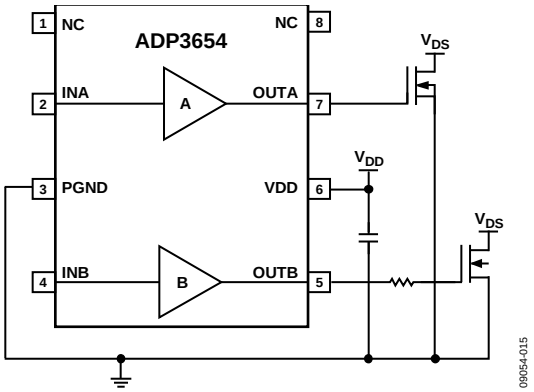

Figure 15. Typical Application Circuit

INPUT DRIVE REQUIREMENTS (INA AND INB)

The ADP3654 is designed to meet the requirements of modern digital power controllers; the signals are compatible with 3.3 V logic levels. At the same time, the input structure allows for input voltages as high as V_{DD}.

An internal pull-down resistor is present at the input, which guarantees that the power device is off in the event that the input is left floating.

LOW-SIDE DRIVERS (OUTA, OUTB)

The ADP3654 dual drivers are designed to drive ground referenced N-channel MOSFETs. The bias is internally connected to the V_{DD} supply and PGND.

When ADP3654 is disabled, both low-side gates are held low. Internal impedance is present between the OUTA pin and GND and between the OUTB pin and GND; this feature ensures that the power MOSFET is normally off when bias voltage is not present.

When interfacing ADP3654 to external MOSFETs, the designer should consider ways to make a robust design that minimizes stresses on both the driver and the MOSFETs. These stresses include exceeding the short time duration voltage ratings on the OUTA and OUTB pins, as well as the external MOSFET.

Power MOSFETs are usually selected to have a low on resistance to minimize conduction losses, which usually implies a large input gate capacitance and gate charge.

SUPPLY CAPACITOR SELECTION

For the supply input (V_{DD}) of the ADP3654, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents that are drawn.

An improper decoupling can dramatically increase the rise times because excessive resonance on the OUTA and OUTB pins can, in some extreme cases, damage the device, due to inductive overvoltage on the VDD, OUTA, or OUTB pin.

The minimum capacitance required is determined by the size of the gate capacitances being driven, but as a general rule, a 4.7 µF, low ESR capacitor should be used. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Use a smaller ceramic capacitor (100 nF) with a better high frequency characteristic in parallel to the main capacitor to further reduce noise.

Keep the ceramic capacitor as close as possible to the ADP3654 device and minimize the length of the traces going from the capacitor to the power pins of the device.

PCB LAYOUT CONSIDERATIONS

Use the following general guidelines when designing PCBs:

- Trace out the high current paths and use short, wide (>40 mil) traces to make these connections.
- Minimize trace inductance between the OUTA and OUTB outputs and MOSFET gates.
- Connect the PGND pin of the ADP3654 device as closely as possible to the source of the MOSFETs.
- Place the V_{DD} bypass capacitor as close as possible to the VDD and PGND pins.
- Use vias to other layers, when possible, to maximize thermal conduction away from the IC.

Figure 16 shows an example of the typical layout based on the preceding guidelines.

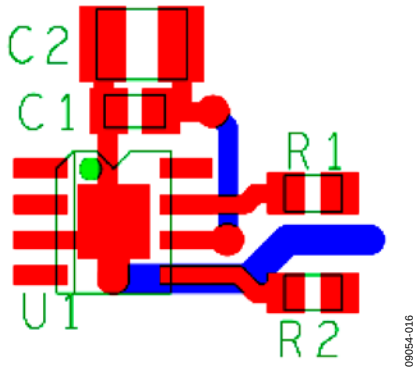

Figure 16. External Component Placement Example

Note that the exposed pad of the package is not directly connected to any pin of the package, but it is electrically and thermally connected to the die substrate, which is the ground of the device.

PARALLEL OPERATION

The two driver channels present in the ADP3654 device can be combined to operate in parallel to increase drive capability and minimize power dissipation in the driver.

The connection scheme is shown in Figure 17. In this configuration, INA and INB are connected together, and OUTA and OUTB are connected together.

Particular attention must be paid to the layout in this case to optimize load sharing between the two drivers.

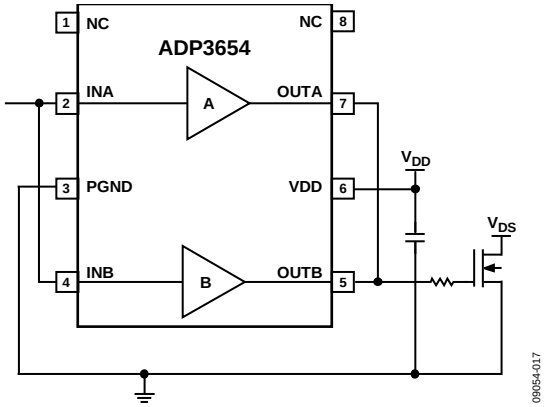

Figure 17. Parallel Operation

THERMAL CONSIDERATIONS

When designing a power MOSFET gate drive, the maximum power dissipation in the driver must be considered to avoid exceeding maximum junction temperature.

Data on package thermal resistance is provided in Table 2 to help the designer with this task.

There are several equally important aspects that must be considered, such as the following:

- Gate charge of the power MOSFET being driven
- Bias voltage value used to power the driver
- Maximum switching frequency of operation
- Value of external gate resistance
- Maximum ambient (and PCB) temperature
- Type of package

All of these factors influence and limit the maximum allowable power dissipated in the driver.

The gate of a power MOSFET has a nonlinear capacitance characteristic. For this reason, although the input capacitance is usually reported in the MOSFET data sheet as C_{ISS}, it is not useful to calculate power losses.

The total gate charge necessary to turn on a power MOSFET device is usually reported on the device data sheet under Q_G. This parameter varies from a few nanocoulombs (nC) to several hundred nC, and is specified at a specific V_{GS} value (10 V or 4.5 V).

The power necessary to charge and then discharge the gate of a power MOSFET can be calculated as:

$$P_{GATE} = V_{GS} \times Q_G \times f_{SW}$$

where:
V_{GS} is the bias voltage powering the driver (VDD).
Q_G is the total gate charge.
f_{SW} is the maximum switching frequency.

The power dissipated for each gate (P_{GATE}) still needs to be multiplied by the number of drivers (in this case, 1 or 2) being used in each package, and it represents the total power dissipated in charging and discharging the gates of the power MOSFETs.

Not all of this power is dissipated in the gate driver because part of it is actually dissipated in the external gate resistor, R_G. The larger the external gate resistor is, the smaller the amount of power that is dissipated in the gate driver.

In modern switching power applications, the value of the gate resistor is kept at a minimum to increase switching speed and minimize switching losses.

In all practical applications where the external resistor is in the order of a few ohms, the contribution of the external resistor can be neglected, and the extra loss is assumed in the driver, providing a good guard band to the power loss calculations.

In addition to the gate charge losses, there are also dc bias losses, due to the bias current of the driver. This current is present regardless of the switching.

$$P_{DC} = V_{DD} \times I_{DD}$$

The total estimated loss is the sum of P_{DC} and P_{GATE}.

$$P_{LOSS} = P_{DC} + (n \times P_{GATE})$$

where n is the number of gates driven.

When the total power loss is calculated, the temperature increase can be calculated as

$$\Delta T_J = P_{LOSS} \times \theta_{JA}$$

Design Example

For example, consider driving two IRFS4310Z MOSFETs with a V_{DD} of 12 V at a switching frequency of 300 kHz, using an ADP3654 in the SOIC_N_EP package.

The maximum PCB temperature considered for this design is 85°C.

From the MOSFET data sheet, the total gate charge is Q_G = 120 nC.

$$P_{GATE} = 12\ V \times 120\ nC \times 300\ kHz = 432\ mW$$

$$P_{DC} = 12\ V \times 1.2\ mA = 14.4\ mW$$

$$P_{LOSS} = 14.4\ mW + (2 \times 432\ mW) = 878.4\ mW$$

The SOIC_N_EP thermal resistance is 59°C/W.

$$\Delta T_J = 878.4\ mW \times 59°C/W = 51.8°C$$

$$T_J = T_A + \Delta T_J = 136.8°C \leq T_{JMAX}$$

This estimated junction temperature does not factor in the power dissipated in the external gate resistor and, therefore, provides a certain guard band.

If a lower junction temperature is required by the design, the MINI_SO_EP package can be used, which provides a thermal resistance of 43°C/W, so that the maximum junction temperature is

$$\Delta T_J = 878.4\ mW \times 43°C/W = 37.7°C$$

$$T_J = T_A + \Delta T_J = 122.7°C \leq T_{JMAX}$$

Other options to reduce power dissipation in the driver include reducing the value of the V_{DD} bias voltage, reducing switching frequency, and choosing a power MOSFET with smaller gate charge.

OUTLINE DIMENSIONS

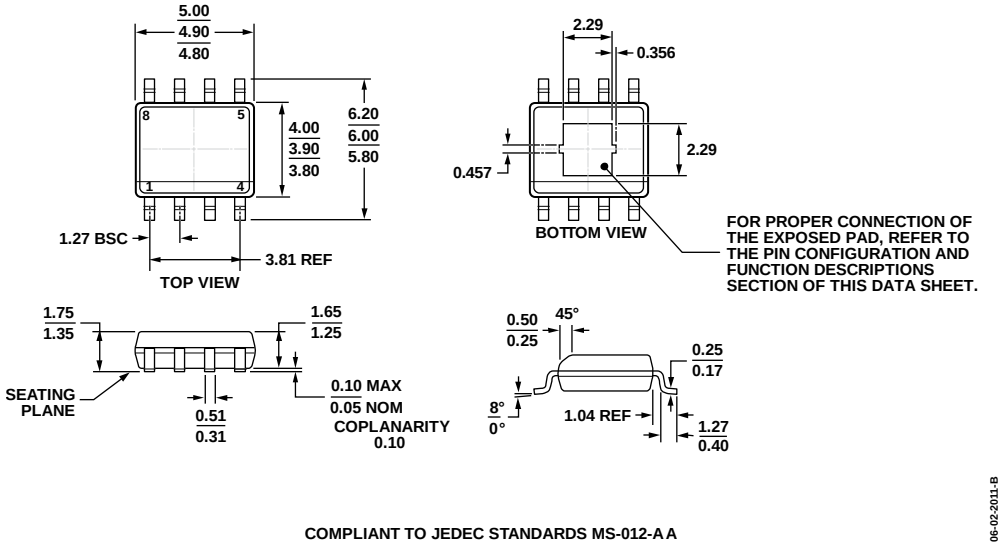

Figure 18. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body (RD-8-1)
Dimensions shown in millimeters

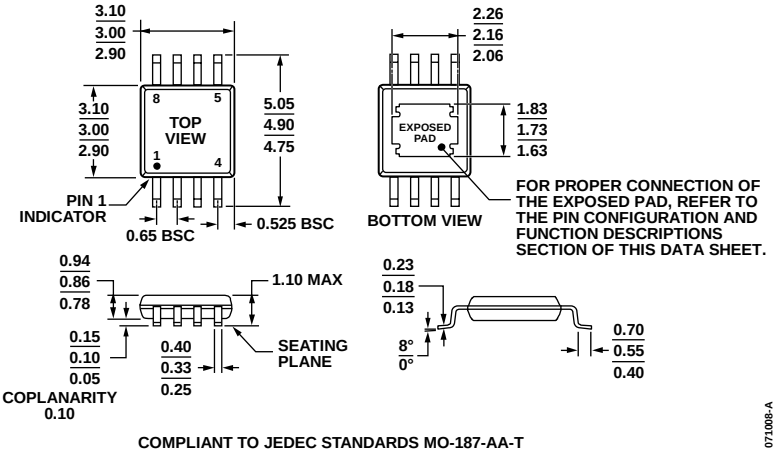

Figure 19. 8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]
(RH-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	UVLO Option	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADP3654ARDZ	4.5 V	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N_EP), Tube	RD-8-1	98	
ADP3654ARDZ-R7	4.5 V	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N_EP), 7" Tape and Reel	RD-8-1	1,000	
ADP3654ARDZ-RL	4.5 V	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N_EP), 13" Tape and Reel	RD-8-1	2,500	
ADP3654ARHZ	4.5 V	−40°C to +125°C	8-Lead Mini Small Outline Package (MINI_SO_EP), Tube	RH-8-1	50	78
ADP3654ARHZ-R7	4.5 V	−40°C to +125°C	8-Lead Mini Small Outline Package (MINI_SO_EP), 7" Tape and Reel)	RH-8-1	1,000	78
ADP3654ARHZ-RL	4.5 V	−40°C to +125°C	8-Lead Mini Small Outline Package (MINI_SO_EP), 13" Tape and Reel	RH-8-1	3,000	78

[1] Z = RoHS Compliant Part.

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