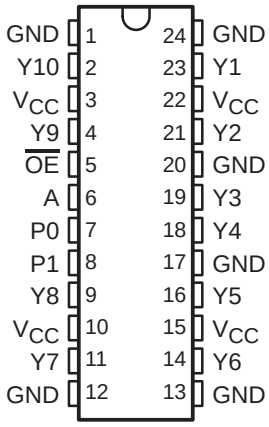
- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **LVTTL-Compatible Inputs and Outputs**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Distributes One Clock Input to Ten Outputs**
- **Outputs Have Internal Series Damping Resistor to Reduce Transmission Line Effects**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**
- **Available in Q-Temp Automotive**
  High Reliability Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC2351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input disables the outputs to a high-impedance state. Each output has an internal series damping resistor to improve signal integrity at the load. The CDC2351 operates at nominal 3.3-V V_{CC}.

The propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part-to-part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC2351 is characterized for operation from 0°C to 70°C. The CDC2351Q is characterized for operation over the full automotive temperature range of –40°C to 125°C.

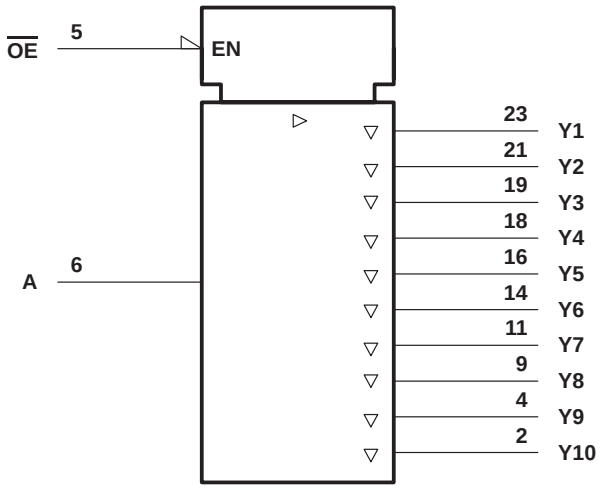
FUNCTION TABLE

INPUTS		OUTPUTS
A	$\overline{OE}$	In
L	H	Z
H	H	Z
L	L	L
H	L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

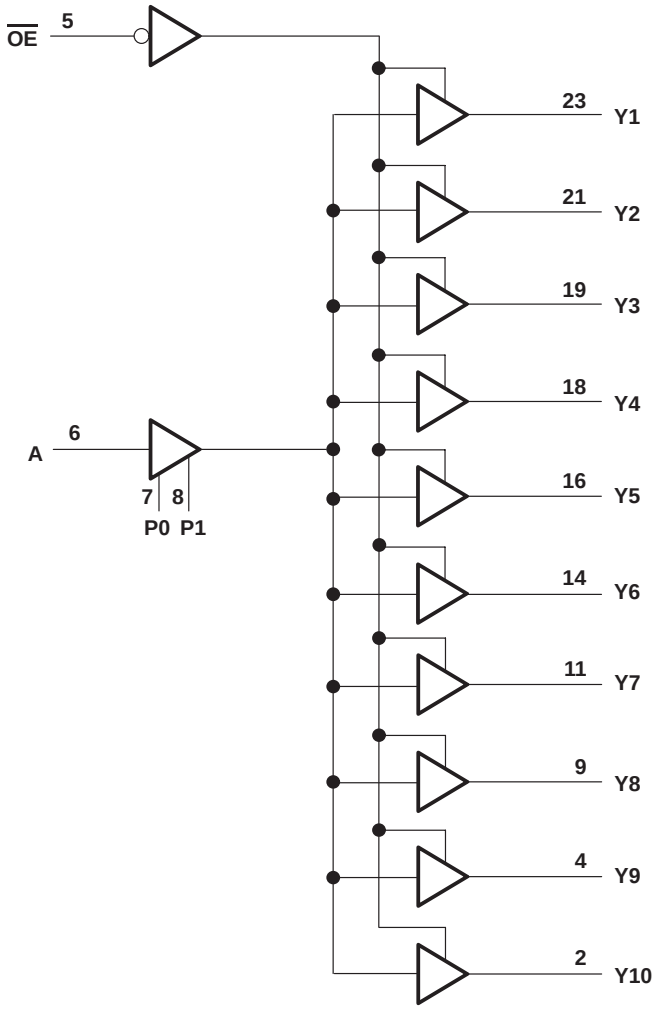
EPIC-IIB is a trademark of Texas Instruments.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,
V_O (see Note 1) . . . . . –0.5 V to 3.6 V
Current into any output in the low state, I_O . . . . . 24 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_I < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.65 W
DW package . . . . . 1.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	5.5	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	CDC2351	0	70	°C
		CDC2351Q	–40	125	

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = – 12 mA		2			V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA				0.8	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	µA
I_O‡	V_{CC} = 3.6 V,	V_O = 2.5 V		–7		–70	mA
I_{OZ}	V_{CC} = 3.6 V,	V_{CC} = 3 V or 0				±10	µA
I_{CC}	V_{CC} = 3.6 V,	I_O = 0, V_I = V_{CC} or GND	Outputs high			0.3	mA
			Outputs low			15	
			Outputs disabled			0.3	
C_i	V_I = V_{CC} or GND,	V_{CC} = 3.3 V,	f = 10 MHz		4		pF
C_o	V_O = V_{CC} or GND,	V_{CC} = 3.3 V,	f = 10 MHz		6		pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

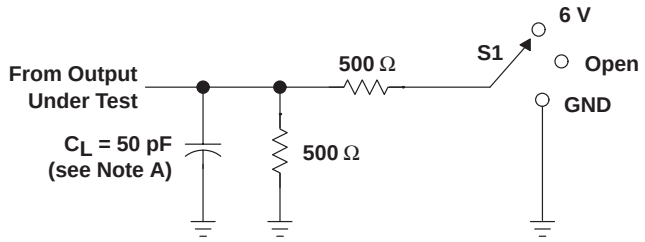
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC2351 V_{CC} = 3.3 V, T_A = 25°C			CDC2351Q V_{CC} = 3 V to 3.6 V, T_A = –40°C to 125°C		CDC2351 V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.8	4.3	4.8	1.1	11			ns
t_{PHL}			3.6	4.1	4.6	1	9.7			
t_{PZH}	$\overline{OE}$	Y	2.4	4.9	6.0	1	12	1.8	6.9	ns
t_{PZL}			2.4	4.3	6.0	1	11.1	1.8	6.9	
t_{PHZ}	$\overline{OE}$	Y	2.2	4.4	6.3	1	11.1	2.1	7.1	ns
t_{PLZ}			2.2	4.6	6.3	1	11.5	2.1	7.3	
$t_{sk(o)}$	A	Y		0.3	0.5		2.5		0.5	ns
$t_{sk(p)}$	A	Y		0.2	0.8		3		0.8	ns
$t_{sk(pr)}$	A	Y			1				1	ns
t_r	A	Y					2.5		2.5	ns
t_f	A	Y					2.5		2.5	ns

switching characteristics temperature and V_{CC} coefficients over recommended operating free-air temperature and V_{CC} range (see Note 4)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$\propto t_{PLH}(T)$	Average temperature coefficient of low to high propagation delay	A	Y		85†	ps/10°C
$\propto t_{PHL}(T)$	Average temperature coefficient of high to low propagation delay	A	Y		50†	ps/10°C
$\propto t_{PLH}(V_{CC})$	Average V_{CC} coefficient of low to high propagation delay	A	Y		–145‡	ps/ 100 mV
$\propto t_{PHL}(V_{CC})$	Average V_{CC} coefficient of high to low propagation delay	A	Y		–100‡	ps/ 100 mV

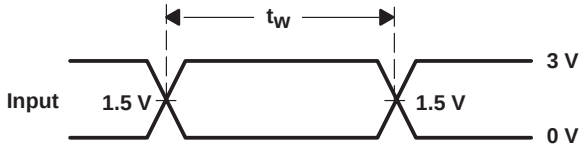
† $\propto t_{PLH}(T)$ and $\propto t_{PHL}(T)$ are virtually independent of V_{CC}.
‡ $\propto t_{PLH}(V_{CC})$ and $\propto t_{PHL}(V_{CC})$ are virtually independent of temperature.
NOTE 4: This data was extracted from characterization material and are not tested at the factory.

PARAMETER MEASUREMENT INFORMATION

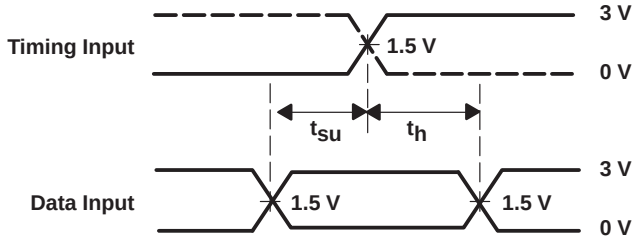


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

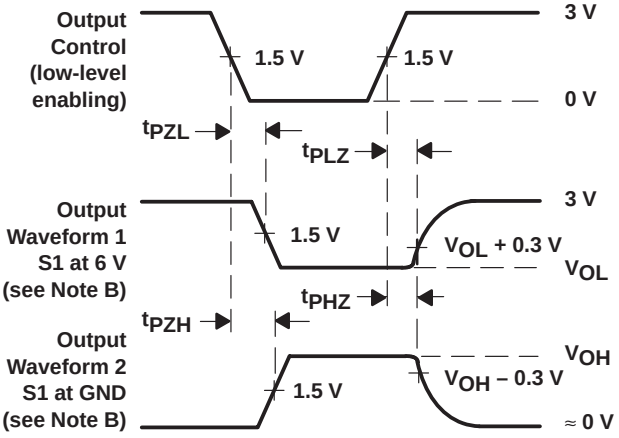
LOAD CIRCUIT



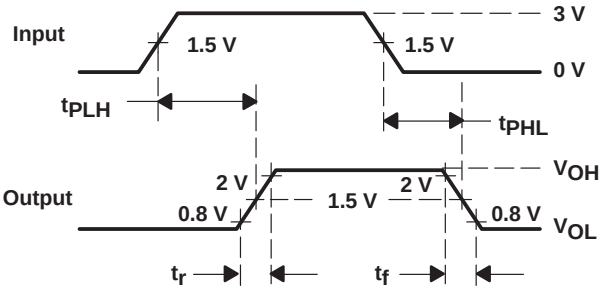
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

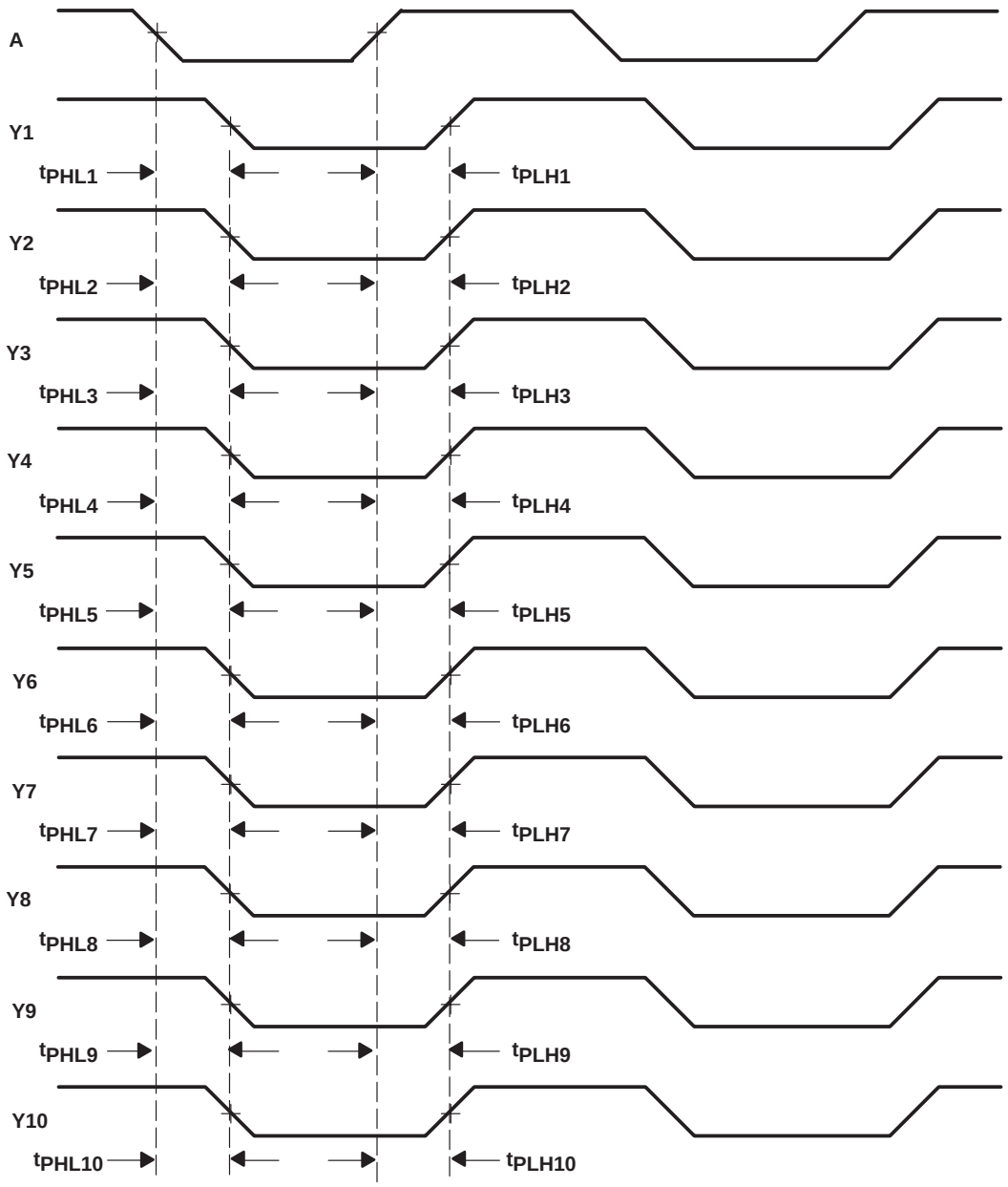


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $| t_{PLHn} - t_{PHLn} |$ (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC2351DB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CK2351	Samples
CDC2351DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CK2351	Samples
CDC2351DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2351	Samples
CDC2351DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2351	Samples
CDC2351DWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC2351	Samples
CDC2351QDB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK2351Q	Samples
CDC2351QDBG4	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK2351Q	Samples
CDC2351QDBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK2351Q	Samples
CDC2351QDBRG4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK2351Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CDC2351, CDC2351-Q1 :

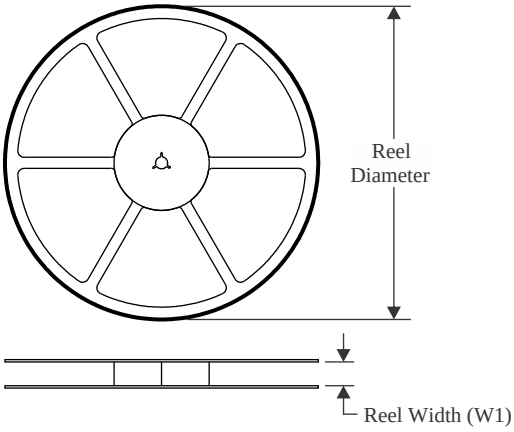
- Catalog : CDC2351
- Automotive : CDC2351-Q1
- Enhanced Product : CDC2351-EP, CDC2351-EP

NOTE: Qualified Version Definitions:

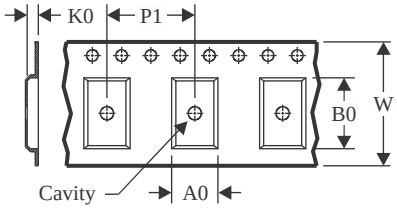
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

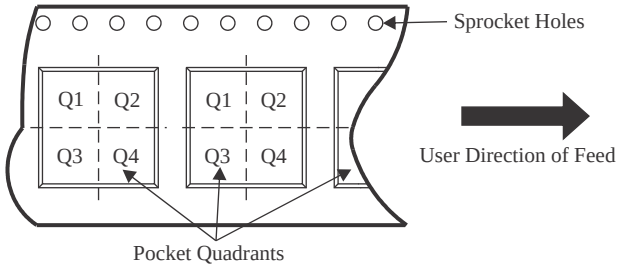


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

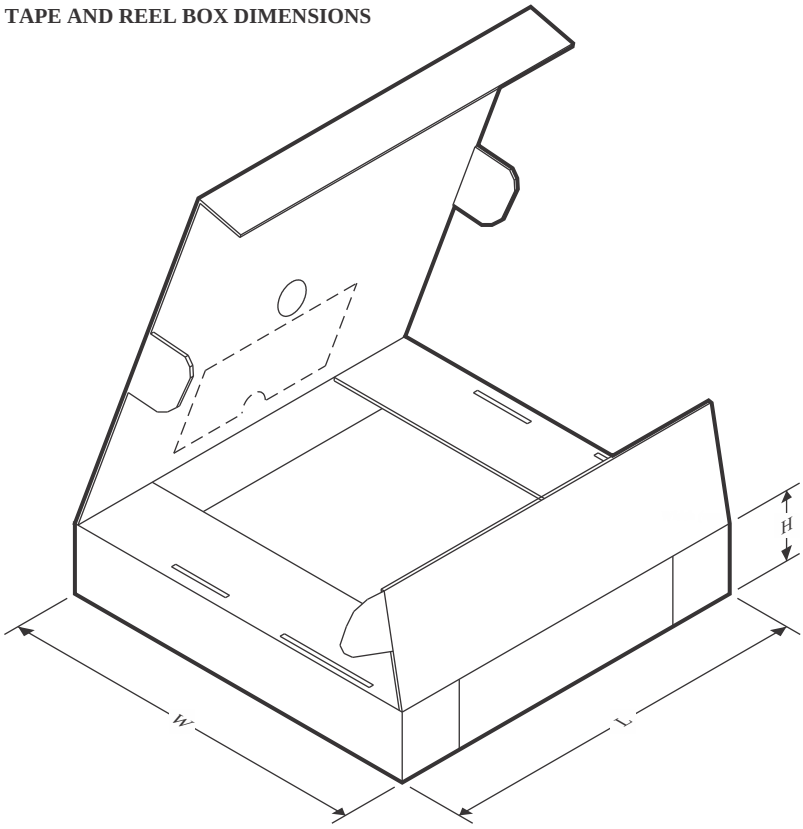
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC2351DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CDC2351DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CDC2351QDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CDC2351QDBRG4	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

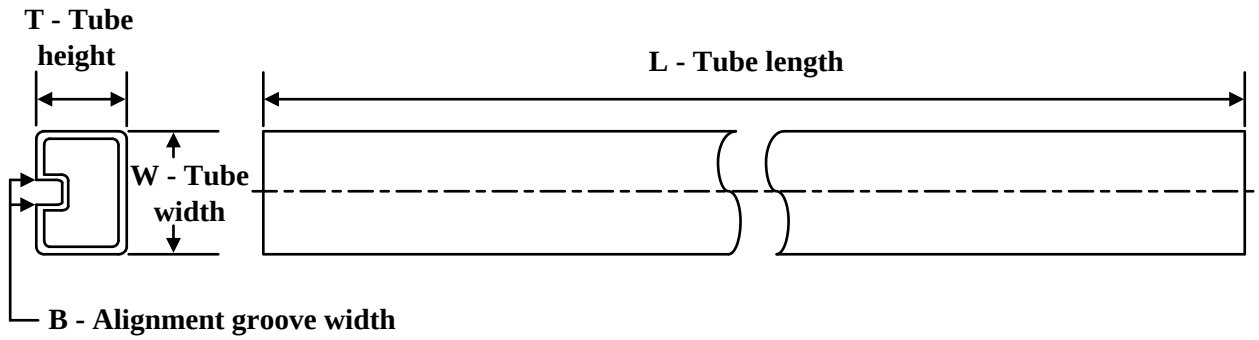
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC2351DBR	SSOP	DB	24	2000	356.0	356.0	35.0
CDC2351DWR	SOIC	DW	24	2000	350.0	350.0	43.0
CDC2351QDBR	SSOP	DB	24	2000	356.0	356.0	35.0
CDC2351QDBRG4	SSOP	DB	24	2000	356.0	356.0	35.0

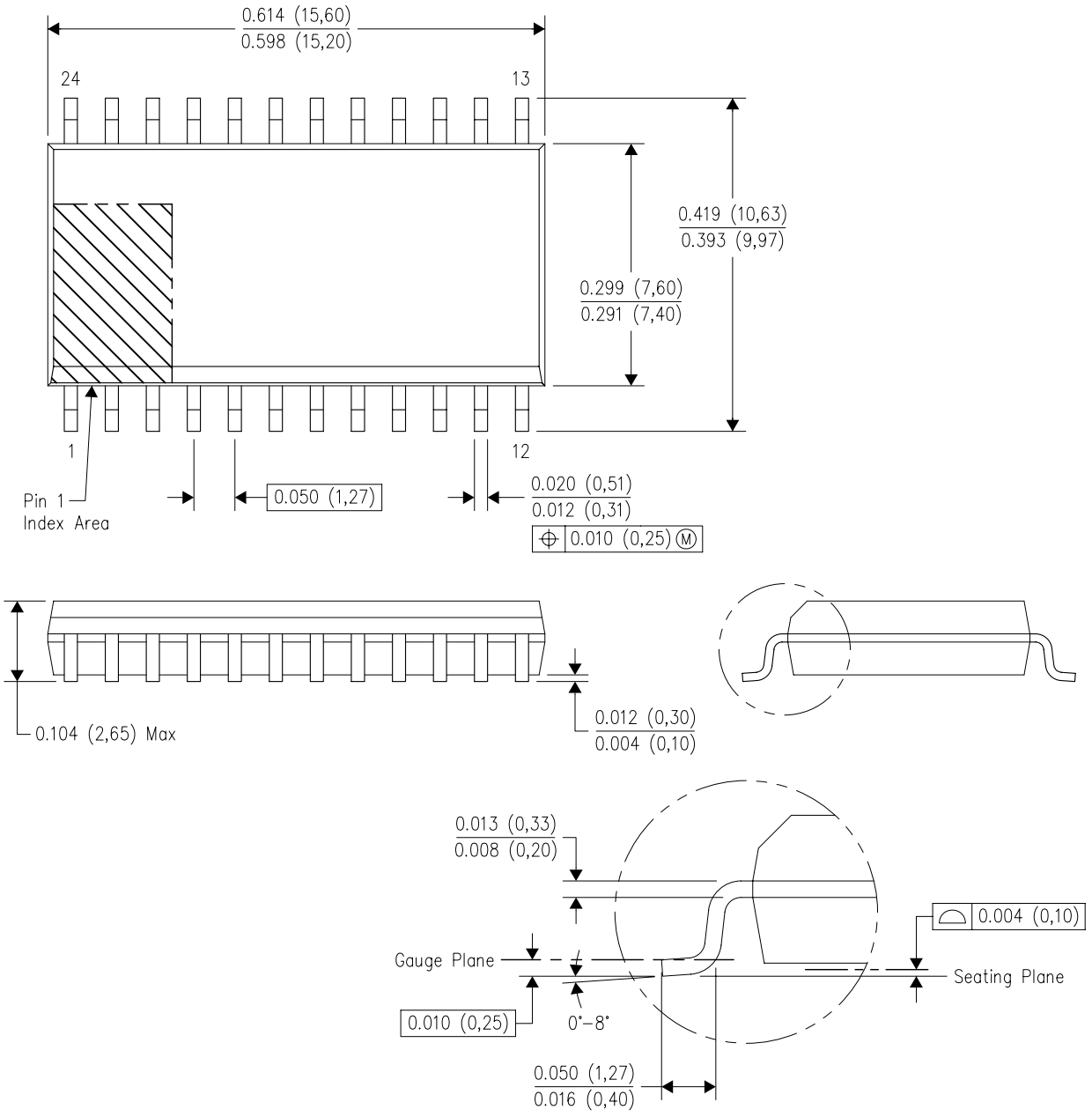
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC2351DB	DB	SSOP	24	60	530	10.5	4000	4.1
CDC2351DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
CDC2351QDB	DB	SSOP	24	60	530	10.5	4000	4.1
CDC2351QDBG4	DB	SSOP	24	60	530	10.5	4000	4.1

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

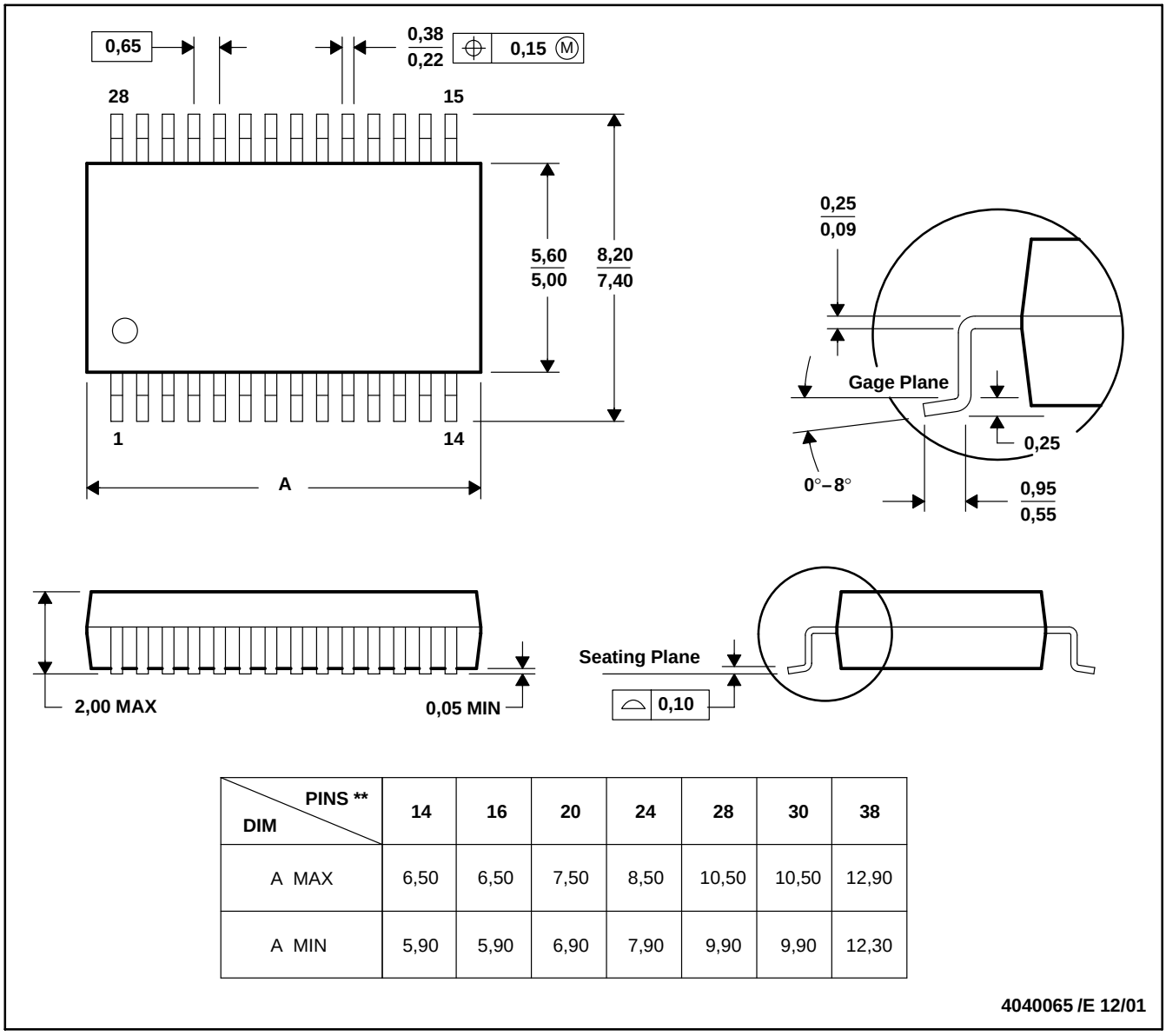


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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